

## Explore the world of ALTERA

The Altera Development Kit (ADK) is the perfect companion for your ALTERA devices and design software. Just *prototype* is not the key word but understanding the Altera PLDs architectures comparison and utilizing the Quartus to its maximum capabilities and potential.

The purpose of ADK is to teach the concepts of VLSI designing with various applications giving complete support for various Altera devices; which makes it ideal choice for design development.

ADK is truly a low cost universal platform for Cyclone, ACEX1K & MAX7000S family of devices, providing pluggable add-on modules for different design requirements.

# ADK



## Your world of Altera



The Altera Development Kit (ADK) is a low cost universal platform for testing and verifying designs based on the Altera PLDs. The purpose of ADK is to teach the concepts of VLSI designing with various applications.

As the ADK gives complete support for various Altera devices and is the ideal choice for project development and verification of designs.

ADK comes along with various adaptors of FPGAs and CPLDs, which are optional to user. Every adaptor is pluggable with baseboard with the help of connectors.



### Features & Specifications

- Multi- device support for Altera PLDs
- Packages supported PLCC84 and TQ144
- Maximum 104 user I/Os
- All I/Os accessible to user through berg pin header
- I/O isolating switches (bug isolators, used for isolating general I/Os from PLD pins, replacement for jumpers)
- Four Multiplexed 7-Segment displays
- User selectable configuration modes, using either JTAG /Passive Slave Serial
- Programming Mode selection header
- Byte-blaster cable interface for configuration of Altera FPGAs/CPLDs
- On board 8-MHz Clock oscillator (user selectable)
- Configurable 24 switches as I/P or O/P
- 16 digital LED indicated outputs
- Power on Reset key. Support for different I/O Standards
- 4 on board push-to-ON keys
- Optically isolated relay card

### Individual Module Specifications

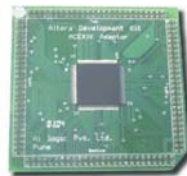
#### **Cyclone FPGA Module**

EP1C3 TC144-8 device.  
2,910 Logic elements (LE).



#### **ACEX1K FPGA Module**

50,000 gate density EP1K50 TC144.  
2,880 Logic elements (LE).



#### **MAX7000s CPLD Module**

EPM7128S LC84-15 device.  
2,500 system gates.  
128 macrocells CPLD.



#### **Relay Module**

Two Optically isolated relays  
NC, NO, COMM I/Os on power header  
Relay ON indication



### Applications

- FPGA based design development
- Access Control System
- Design of 8/16/24/32 bit Counters
- 8/16/24/32 bit Shift Registers
- Timer Designs IC8254 and IC8253
- 8255 PPI Design
- 4-bit and 8-bit ALUs
- All Digital Logic Gates and Functions